Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original) A method of tetrahedral interpolation, comprising the steps of:

(a) receive a color space input point;

(b) compute a base point and three differentials for said input point;

(c) compare said three differentials;

(d) compute tetrahedron vertices from the results of steps (b) and (c), a first one of said vertices being said base point;

(e) find output values for each of said vertices;

(f) compute an interpolated output value for said input point as the sum of the output value of said base point plus the inner product of said differentials in size order with corresponding differences of said output values for said vertices.

Claim 2 (original) The method of claim 1, wherein:

(a) said output values of step (e) are a single color value for each vertex.

Claim 3 (original) The method of claim 1, wherein:

(a) said output values of step (e) are three color values for each vertex.

Claim 4 (original) The method of claim 1, wherein:

(a) said output values of step (e) are four color values for each vertex.

Claim 5 (original) The method of claim 1, wherein:

(a) said output values of step (e) are six color values for each vertex.

Claim 6 (original) A tetrahedral interpolation system, comprising:

(a) an input for receiving an input point;

(b) first circuitry coupled to said input and arranged to output a base point plus three differentials for said input point, said differentials sorted in size order;

(c) second circuitry coupled to an output of said first circuitry and to compute lookup table addresses of four vertices of an interpolation tetrahedral for said input point;

(d) four memory banks containing said lookup table and coupled to said second circuitry, wherein each of said memory banks contains entries for all addresses with a common residue modulo 4; and

(e) third circuitry coupled to said four memory banks and said first circuitry, said third circuitry arranged to compute a tetrahedral interpolation value for said input point.